Analog/RF Design Techniques for High Performance Nanoelectronic On-Chip Interconnects

Bao Liu
Electrical and Computer Engineering Department
University of Texas, San Antonio, TX 78249
Email: bliu@utsa.edu

Abstract
On-chip interconnects form the bottleneck of VLSI system performance. As technology progresses, VLSI on-chip interconnects encounter increasingly significant challenges, such as (1) signal attenuation and (2) crosstalk coupling. This paper proposes two analog/RF design techniques for high performance nanoelectronic on-chip interconnects: (1) application of distributed amplifiers for signal attenuation compensation by reducing interconnect effective resistance, and (2) application of bandpass filters for noise immunity in a frequency separated VLSI on-chip communication system. HSPICE-RF simulation results in 65nm CMOS technology verify that the proposed analog/RF design techniques achieve improved performance and reliability for high performance nanoelectronic on-chip interconnects.

1 Introduction
Since VLSI process technology scales into the deep submicron domain, VLSI on-chip global interconnects have been the bottleneck of achieving high performance, low power, and reliable VLSI systems. VLSI technology scaling has been dramatically increasing VLSI on-chip interconnect unit length resistance, capacitance, and inductance, leading to significant performance, power consumption, and signal reliability degradation. Two outstanding challenges facing VLSI on-chip interconnects are (1) signal attenuation, and (2) crosstalk coupling.

Signal attenuation comes from dramatic increase of on-chip interconnect resistance in VLSI technology scaling due to geometry shrinking and skin effect. For example, without reverse scaling interconnect resistance becomes more than doubled as VLSI technology migrates from the 90nm node to the 65nm node [5]. In nanotechnology, single walled carbon nanotube resistance includes a series ballistic resistance $R_s \approx 6.5k\Omega$, besides contact and distributed resistances, and additional resistance increase due to current saturation [8]. The resultant resistance shielding effect significantly degrades signal propagation delay and signal transition time along interconnects.

Another significant challenge for VLSI on-chip interconnects is crosstalk coupling. Shielding is more effective a technique for capacitive coupling than inductive coupling among interconnects. As circuit operation frequency increases, inductive coupling increases as well, which significantly compromises reliability and increases design complexity for nanoelectronic systems.

As a result, new design techniques are much needed for VLSI on-chip interconnects in nanotechnology domain. Increasing circuit operation frequency, shrinking signal swing, increasingly significant signal integrity effects and process variations all suggest application of analog and radio frequency design techniques to VLSI digital circuits in nanotechnology domain. This paper explores this possibility, especially, application of two analog/RF design techniques as follow.


2. Application of bandpass filters for coupling noise filtering and reliability improvement in a frequency separated VLSI on-chip communication system.

These techniques have been developed and applied to analog/RF design. Recent technology development has enabled on-chip implementation of these components. This paper proposes application of these techniques for high performance nanoelectronic on-chip interconnects, and present HSPICE-RF simulation results based on 65nm CMOS technology which verify the effectiveness of the proposed techniques. The proposed analog/RF on-chip interconnects can be fabricated in a standard CMOS process at low cost, with reasonable robustness and ease of process control. We expect VLSI technology scaling and/or nanotechnology development enable practical application of the proposed analog/RF on-chip interconnects.

The rest of this paper is organized as follows. Section 2 presents theoretical analysis and progressive design techniques leading to the proposed analog/RF design techniques for high performance nanoelectronic on-chip interconnects. Section 3
presents implementation and simulation results for the proposed techniques, before Section 4 concludes this paper.

2 Analog/RF Design Techniques for High Performance On-Chip Interconnects

We start with an analysis of transmission lines, and present progressive design techniques for high performance nanoelectronic on-chip interconnects leading to the two analog/RF design techniques which this paper proposes.

2.1 Transmission Line Interconnects

As technology scales, and signal wavelengths approach interconnect lengths, interconnects need to be taken as transmission lines, with properly matched load impedance for maximum signal propagation energy efficiency. Signal attenuation remains a serious challenge in impedance matched transmission lines under current technology scaling trend and available nanotechnology techniques. For example, in a distortion-less ($R = L = G = C$) transmission line (series resistance per unit length $R$, series inductance per unit length $L$, shunt conductance per unit length $G$, and shunt capacitance per unit length $C$), signal propagation is given by

$$V(z) = V_0 e^{-\sqrt{RG}z} e^{-j\omega LCz}$$

Signal attenuation $\sqrt{RG}$ is determined by the manufacturing technology (including interconnect height and inter-layer-dielectric thickness) and is independent on interconnect width. Consequently, design techniques are much needed for reduced effective interconnect resistance.

2.2 Buffer Insertion in Conventional Interconnects

Buffers (repeaters and inverters) have traditionally been inserted in long VLSI on-chip interconnects for performance improvement, signal transition time bound, and crosstalk coupling noise reduction. However, its performance improvement is limited by additional capacitance and signal propagation delay introduced by inserted buffers. As technology scales, on-chip interconnect resistance approaches buffer driving resistance, and on-chip interconnect capacitance approaches buffer input capacitance, buffer insertion becomes less effective in nanoelectronic designs.

2.3 Sense Amplifiers in Low Swing Differential Interconnects

VLSI supply voltage scaling and power consumption constraint imply low swing signaling in nanotechnology domain. Differential low swing signaling offers the minimum power consumption and maximum noise immunity [11], wherein two interconnects routing parallel in close proximity carry two opposite signals, the difference between the two signals are captured at the receiver, e.g., by a differential transistor pair (Fig. 1) [6, 9]. Differential signaling achieves significant noise immunity improvement by common noise rejection. The low signal swing and the minimum current loop formed by the differential interconnects also lead to minimum inductive coupling noise to neighboring interconnects. This technique has been widely applied to board level interconnects, and finds increasing applications in on-chip interconnect design. However, performance and reliability remain serious challenges for low swing differential signaling.

2.4 Distributed Amplifiers in Transmission Lines

As VLSI technology scales into nanotechnology domain, interconnects become transmission lines, analog/RF design techniques become applicable to general digital circuits. For example, distributed circuit design is an emerging trend for analog/RF circuits [4], which include interconnect transmission lines as an integral part of analog/RF circuits. Distributed amplifiers absorb intrinsic transistor capacitors into the transmission lines, allowing them to exceed the typical bandwidth limit due to intrinsic transistor capacitors, and achieve larger-than-usual gain-bandwidth product.

Distributed amplifiers [3, 7] consist of a series of amplifiers between a pair of transmission lines. Conventional distributed amplifiers are built on common-source transistors [7], differential distributed amplifiers can be built on differential transistor pairs, similar to those in common operational amplifiers (Fig. 2) [3]. The RF signal at the input transmission line is taken as input by the distributed amplifiers and amplified to the output transmission line. The signal at the input transmission line attenuates while the signal at the output transmission line strengthens. In order to control the voltage swing, the output transmission line has its inductance decreases as the signal...
distributed amplifiers in transmission lines are verified by simulation global interconnect resistance is 40 Ω/µm.

To suppress coupling noise, this paper further proposes application of bandpass filters in nanotechnology VLSI circuits and on-chip communication systems to capture signals at specific frequencies. This implies frequency separation, e.g., to transmit signals at different carrier frequencies in different on-chip interconnects. This is easily implementable in modern VLSI designs, where the frequency of a data signal is largely given by its clock signal. The increasing number of clock domains or clock frequencies in modern VLSI designs increases the effect of bandpass filters.

Recent progress has enabled integration of RF bandpass filters at low cost in standard CMOS process [2]. This is achieved by employing new circuit topologies, e.g., Gyrators or active inductors built on standard CMOS transistors significantly reduces chip area requirement for inductors [10], based on which Q-enhanced LC filters achieve higher operational frequencies and are less sensitive to parasitic capacitance compared with the traditional active RC, MOSFET-C, and Gm-C bandpass filters [2].

3 Implementation and Simulation

3.1 Distributed Amplifiers

This section presents HSPICE-RF simulation results which verify the proposed analog/RF design techniques for high performance nano electronic on-chip interconnects. The proposed distributed amplifiers in transmission lines are verified by simulation in 65nm CMOS technology [1], wherein the typical global interconnect resistance is 40.8Ω/µm, capacitance (including ground and fringe) 148.0fF/µm, and inductance 0.5pH/µm.

Single stage common-source amplifiers are implemented in the form of common inverters in 65nm CMOS technology. The gate of the common-source amplifier transistors are biased at 0.45V under 1V supply voltage. Two such amplifiers are included at the head and at the center of two input and two output 100μm transmission lines. HSPICE-RF simulation results show that these distributed amplifiers achieve reduced signal propagation delay across the transmission lines and reduced output signal transition times, as well as increased output signal swing, at the cost of 8.84μW power consumption, and moderate chip area with 24μm transistor width for the inverter amplifiers (Table 1).

<table>
<thead>
<tr>
<th></th>
<th>W (µm)</th>
<th>A</th>
<th>B (MHz)</th>
<th>P (µW)</th>
<th>D (ns)</th>
<th>Tr (ns)</th>
<th>Sw (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>28.76</td>
<td>49.25</td>
</tr>
<tr>
<td>II</td>
<td>24</td>
<td>8.84</td>
<td>8.59</td>
<td>36.31</td>
<td>10.92</td>
<td>8.41</td>
<td>1.11</td>
</tr>
</tbody>
</table>

Table 1: Transistor width W, DC gain A, unit gain bandwidth B, power consumption P, transmission line delay D, output signal transition time Tr, and output signal voltage swing Sw for 4 100μm long transmission lines in 65nm CMOS technology driven by ramp input signals of 1mV swing and 10ps transition time with (I) no amplifier, and (II) 2 distributed amplifiers, respectively.

3.2 Bandpass Filter

The proposed bandpass filter technique is verified by HSPICE-RF simulation in 65nm CMOS process for an active inductors based Q-enhanced LC bandpass filter (Fig. 3) [10]. The filter is in a symmetric differential structure, including two active inductors and a negative resistor. The active inductors are formed by two cascaded PMOS transistors (M11a and M2a), or M1b and M2b), of which the input impedance (from the source of gate M2a) is given by $Z_{in} = \frac{V_{in}}{I_{in}} = \frac{C_{gs1}}{g_m1g_m2}$ where $C_{gs1}$ is the gate-source capacitance of transistor $M_{1a}$, $g_m1$ and $g_m2$ are the transconductances of transistors $M_{1a}$ and $M_{2a}$, respectively. The negative resistor is formed by the cross-connected differential transistor pair (M11a and M11b), of which resistance is given by $R = \frac{V}{I} = \frac{g_m}{g_m}$ where $g_m$ is the transconductance of the identical transistors $M_{1a}$ and $M_{1b}$. The common gate transistors $M_1$ and $M_2$ are input buffers. The main characteristics and the frequency response of this bandpass filter are given in Table 2 and Fig. 4, respectively.

4 Conclusion

This paper proposes application of analog/RF design techniques for high performance nano electronic on-chip intercon-
Figure 3: An active inductors based Q-enhanced LC bandpass filter.

Table 2: Transistor width W, maximum gain A at the center frequency $F_c$, 3dB bandwidth $B_3$, quality factor $Q$, total current $I_{total}$, and output signal voltage swing $S$ of a Q-enhanced LC bandpass filter driven by input signals of 1mV swing and 10ps transition time in 65nm CMOS technology.

<table>
<thead>
<tr>
<th>W (µm)</th>
<th>A (dB)</th>
<th>$F_c$ (GHz)</th>
<th>$B_3$ (GHz)</th>
<th>$Q$ (-)</th>
<th>$I_{total}$ (µA)</th>
<th>$S$ (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2</td>
<td>24.98</td>
<td>4.69</td>
<td>0.02</td>
<td>234.50</td>
<td>125.64</td>
<td>31.30</td>
</tr>
</tbody>
</table>

nects. As technology progresses, on-chip interconnects need to be modeled as transmission lines, where signal attenuation and crosstalk coupling remain serious challenges. This paper proposes application of distributed amplifiers for signal attenuation compensation, and bandpass filters for noise immunity in a frequency separated communication system. HSPICE-RF simulation results in 65nm CMOS technology verify that the proposed techniques achieve improved performance and reliability for high performance nanoelectronic on-chip interconnects. We expect VLSI technology scaling and/or nanotechnology development enable practical application of the proposed techniques.

Figure 4: Gain vs. input signal frequency for the bandpass filter in Fig. 3.

References


